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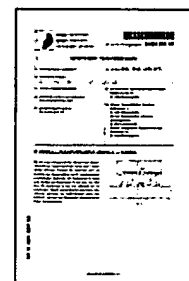
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Hauer, Heiner, Dipl.-Ing.;
Spatscheck, Thomas, Dipl.-Ing.;Assignee: **ANT Nachrichtentechnik GmbH**
[News, Profiles, Stocks and More about this company](#)Published / Filed: **Jan. 2, 1992 / March 23, 1991**Application Number: **EP1991000104586**IPC Code: **H01L 21/60; H01L 23/13;**Priority Number: **June 23, 1990 DE1990004020048**

Abstract:


An arrangement comprising substrate and component in which the component is permanently joined to the substrate by means of a soldering operation has projections (5) either on the substrate (2) at the point provided for the component or on the component (3) itself, or both on the component (3) and on the substrate (2). The projections (5) are outside the surfaces (1, 1') to be soldered and their extension perpendicular to the substrate plane is determined by the distance (hs) required between substrate and component.

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Legal Status:

Designated Country: **BE FR GB IT NL SE**

Family:




PDF	Publication	Pub. Date	Filed	Title
	JP4233294A2	Aug. 21, 1992	June 20, 1991	DEVICE HAVING BOARD AND UNIT
	EP0463297A1	Jan. 2, 1992	March 23, 1991	Arrangement comprising substrate and component and method of making the same
	DE4020048A1	Jan. 2, 1992	June 23, 1990	ANORDNUNG AUS SUBSTRAT UND BAUELEMENT UND VERFAHREN ZUR

			HERSTELLUNG
3 family members shown above			

First Claim: Show all claims

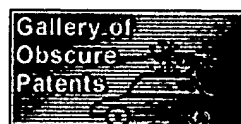
1. Anordnung aus Substat und Bauelement wobei das Bauelement mittels eines Lötvorganges mit dem Substrat fest verbunden wird, dadurch gekennzeichnet, daß entweder am Substrat (2) an der für das Bauelement (3) vorgesehenen Stelle oder am Bauelement (3) selbst oder sowohl am Bauelement (3) als auch am Substrat (2) Vorsprünge (5) vorgesehen sind, die sich außerhalb der zu verlötenden Flächen (1,1') befinden und deren Ausdehnung senkrecht zur Substratebene durch den zwischen Substrat und Bauelement geforderten Abstand (h_s) bestimmt ist.

Forward
References:

PDF	Patent	Pub.Date	Inventor	Assignee	Title
	US6121062	2000-09-19	Karasawa; Kazuaki	Fujitsu Limited	Process of fabricating semiconductor unit employing bumps to bond two components
	US6070788	2000-06-06	Zakel; Elke	Fraunhofer-Gesellschaft zur Förderung der angewandten Forschung e.V.	Method of soldering terminal faces, as well as a method of manufacturing a solder alloy
	US5796123	1998-08-18	Salbreux; Jean-Claude	SGS-Thomson Microelectronics S.A.	Semiconductor component mounted by brazing

Other Abstract
Info:

None



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Buy Now: [More choices...](#)Tools: Add to Work File: [Create new Work File](#) ☒ [Go](#)View: [INPADOC](#) | Jump to: [Top](#) ☒ Go to: [Derwent...](#)☒ [Email this to a friend](#)Title: **JP4233294A2: DEVICE HAVING SUBSTRATE AND UNIT**Country: **JP** JapanKind: **A**Inventor: **KUKE ALBRECHT DR;
HAUER HEINER;
SPATSCHECK THOMAS;**[No Image](#)Assignee: **ANT NACHRICHTENTECH GMBH**
[News, Profiles, Stocks and More about this company](#)Published / Filed: **Aug. 21, 1992 / June 20, 1991**Application Number: **JP1991000148325**IPC Code: **H05K 1/18; H05K 3/24; H05K 3/34;**Priority Number: **June 23, 1990 DE1990004020048**

Abstract:


PURPOSE: To provide a device having a substrate and a unit fixed thereto that the location of the unit is adjustable at an extreme accuracy in a lateral and vertical directions to the plane of the substrate.

CONSTITUTION: Protrusions 5 are provided at regions of a substrate 2 considered for a unit 3 or on the unit itself or both the substrate and unit, and locate at the outside of the surface to be brazed. The sizes of the protrusions in the vertical direction are specified by required distance h3 between the substrate and the unit.

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3 family members shown above				

Other Abstract **DERABS G92-008415**

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